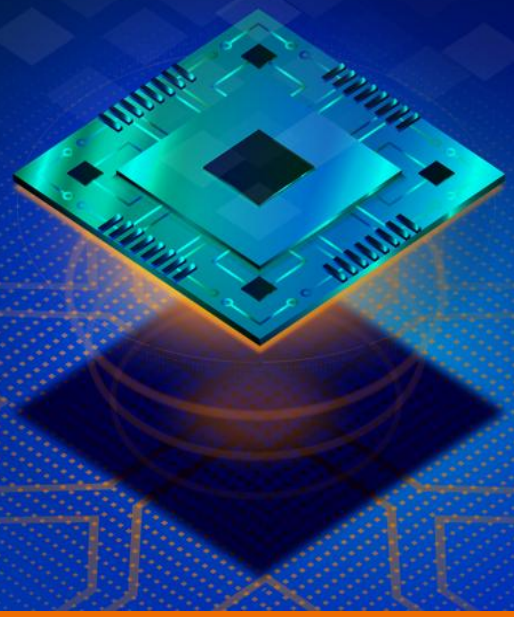


SHINE Singapore Hybrid-Integrated Next-Generation μ-Electronics Centre

7th Technical Workshop

3 February 2026

8:45 am to 6:00 pm

Hosted by:

NUS National University of Singapore | College of Design and Engineering

NUS National University of Singapore · NANYANG TECHNOLOGICAL UNIVERSITY SINGAPORE · NRF SINGAPORE · FSTD OPS-TECH + FUTURE-READY · DSO NATIONAL LABORATORIES · A*STAR Agency for Science, Technology and Research SINGAPORE

Contents

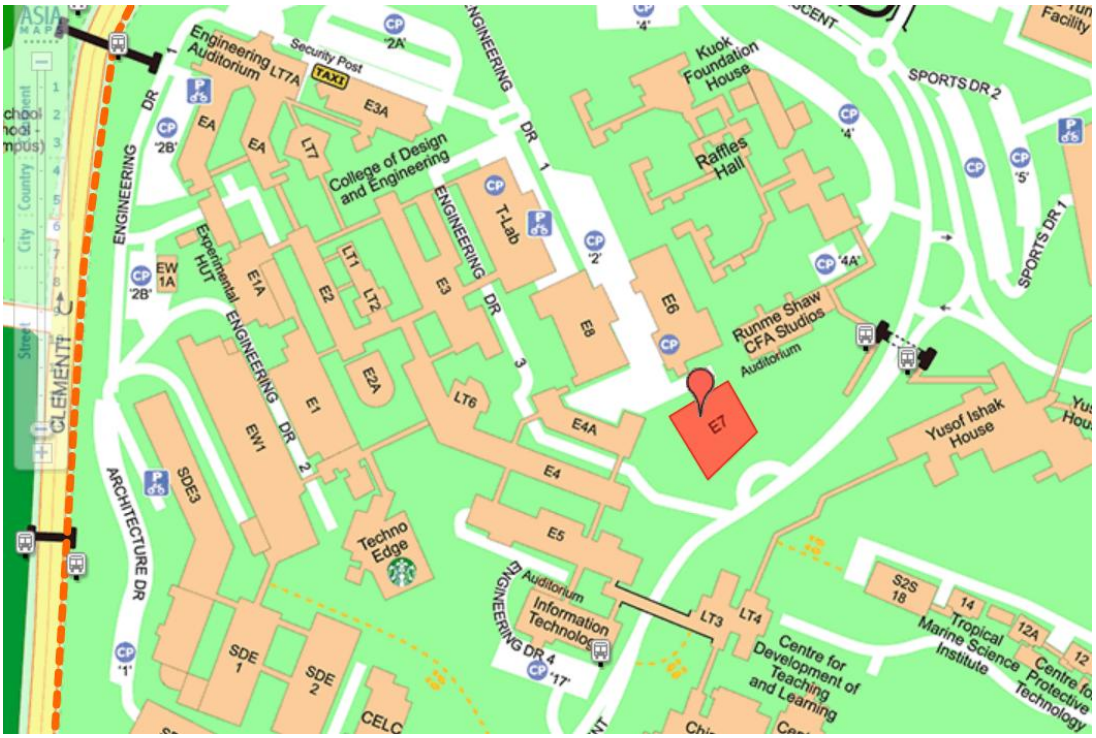
General Information

ORGANIZER

SHINE Programme Management Team
Block E6, #E6-05-03, 5 Engineering Drive 1
Singapore 117608
Tel: (65) 6601 8522
Email: shine@nus.edu.sg
Web: https://shine.nus.edu.sg

VENUE

National University of Singapore
Block E7, Level 3
15 Kent Ridge Crescent
Singapore 119276



(Driver is advised to enter via Engineering Drive 1 and park at Car Park C at Block E6)

The Agenda
- Open Seminar -

SHINE 7th Technical Workshop 3 Feb 2026 E7-03-09 Seminar Room 4			
Open Seminar - Invited Talk			
Start Time	**End Time**	**Presentation Topic**	**Presenter**
8:15 AM	8:45 AM	Registration	
8:45 AM	8:50 AM	Welcome Address	Prof Aaron Thean Director, SHINE Centre National University of Singapore
8:50 AM	9:10 AM	SHINE Programme Update	Prof Lim Yeow Kheng Programme Director, SHINE Centre National University of Singapore
9:10 AM	9:40 AM	Two-Dimensional Materials as Platforms for Scalable Nanoelectronics and Monolithic-3D Integration	Prof Kaustav Banerjee Electrical and Computer Engineering Department University of California, USA
9:40 AM	10:10 AM	Optical Connectivity Technology Challenges in the AI Era	Prof Radha Nagarajan Visiting Professor of NUS SVP and CTO, Optical Engineering Marvell Technology, Inc
10:10 AM	10:40 AM	Strategic Directions for Electronics Packaging	Prof Subramanian S. Iyer Distinguished Professor Charles P. Reames Endowed Chair Electrical Engineering Department University of California, USA
10:40 AM - 11:00 AM | Networking & Break			
11:00 AM	11:30 AM	The Backend Revolution - How Advanced Packaging & Interconnect Redefines Microelectronics	Dr Alfred Yeo Director, Research and Development STATS ChipPAC
11:30 AM	12:00 PM	Memory Matters! Advanced Packaging Roadmap for DRAM and NAND enabling Heterogeneous Integration	Dr Shyam Surthi Distinguished Member of Technical Staff NAND Process Integration Micron Technology, Inc
12:00 PM	12:30 PM	Advanced Laser Integration and Packaging Technologies for High-Performance Silicon Photonic Modules	Dr Jack Sheng Kee Senior Director, Silicon Photonics Business Division Delta Electronics
12:30 PM - 1:30 PM | Lunch			

Agenda
- Technical Workshop -
(For Consortium Members only)

Technical Workshop
**For Consortium Members only*

1:30 PM	2:00PM	What are Quantum Computers and What is the Role of Semiconductors in This Field	Prof Alberto Sangiovanni-Vincentelli SHINE Thrust-1 Research Collaborator University of California, Berkeley, USA
2:00PM	2:30PM	2D Materials Based Composites for Flexible Sensors and Thermal Management	Prof Lee Pooi See SHINE Thrust-2 Co-Investigator Nanyang Technological University
2:30PM	3:00PM	Advanced Materials and Interfaces for Heterogeneous Integration	Dr Li Yanzhen SHINE Thrust-2 Research Fellow Nanyang Technological University
3:00PM	3:30PM	SHINE Design Enablement and Innovation: Learnings from Chiplets to Methodologies	Prof Massimo Alioto SHINE Thrust-1 Co-Investigator National University of Singapore
3:30 PM	4:00 PM	Thermal Malmanagement Solutions for Flexible Antenna Array	Dr Jiang YiZhou SHINE Thrust-3A Research Fellow National University of Singapore
4:00 PM - 4:15 PM: Networking & Break			
4:15 PM	4:45 PM	Flexible Phased Array Demonstrators	Prof Koenraad Mouthaan SHINE Thrust-3B Co-Investigator National University of Singapore
4:45 PM	5:15 PM	Design and Development of the Si/SIC interposer	Dr Lim Teck Guan Senior Scientist (System-in-Package) *A* STAR IME*
5:15 PM	5:45 PM	3D-Printed Micro-Optics for Laser Chip Packaging and Integration	Dr Chua Yun Da SHINE Thrust-4 Research Fellow National University of Singapore
5:45 PM	5:50 PM	Closing Address	Prof Lim Yeow Kheng Programme Director, SHINE Centre National University of Singapore
End of Programme			

Welcome Address

Prof Aaron Thean
Deputy President (Academic Affair) and Provost,
National University of Singapore
Director, SHINE Research Centre

Abstract:

In the welcome address, Prof Aaron will reflect on SHINE Centre's journey since 2021 as a national R&D centre advancing heterogeneous integration. He will highlight SHINE's unique role in bridging materials, processes, and design to enable next-generation microelectronics and emerging applications. As SHINE approaches the successful conclusion of its current phase in June 2026, he will offer a forward-looking glimpse into the Centre's next stage — setting the tone for how SHINE will evolve, scale its impact, and continue strengthening industry collaboration and innovation in hybrid-integrated microelectronics.

Biography:

Aaron Thean is the Globalfoundries Professor of Electrical and Computer Engineering at the National University of Singapore (NUS). He is also the Deputy President (Academic Affairs) and Provost at NUS. In addition to his administrative duties, he is also the Director of SHINE research centre on Next-Generation Hybrid Electronics, where the Heterogeneous Integration process and design are investigated to enable new system innovation by chip packaging and other additive processing.

Prior to NUS, Aaron Thean was the Vice President of Logic Technologies at IMEC, where he directed the research and development of next-generation semiconductor technologies and emerging nano-device architectures. Prior to joining IMEC in 2011, he worked at Qualcomm's CDMA Technologies in San Diego, California. Aaron and his group worked on Qualcomm's 20nm and 16nm mobile System-On-Chip technologies. From 2007 to 2009, Aaron was with IBM, where he developed the 28-nm and 32-nm low-power bulk CMOS technologies at IBM's East Fishkill, New York, facility. Aaron graduated from the University of Illinois at Champaign-Urbana, USA, where he received his B.Sc. (Highest Honours), M.Sc., and PhD. degrees in Electrical Engineering (Edmund J. James Scholar). Recognised by Singapore's National Research Foundation (NRF) as an NRF Returning Singaporean Scientist, he returned to Singapore to pursue his career as an academic in 2016. He has co-authored over 300 technical papers in the areas of advanced microelectronics and holds more than 50 US patents. He is also a Fellow of the US Academy of Inventors.

Programme Highlights

SHINE Programme Update

Prof Lim Yeow Kheng
Programme Director, SHINE Centre
National University of Singapore

Abstract:

Prof Lim will present key programme developments, highlighting collaborations with SHINE Consortium stakeholders and research partners across NUS, NTU, A*STAR-IME, DSO National Labs, and SIMTech. He will share how SHINE's national heterogeneous integration pilot capabilities support practical "mix-and-match" hybrid technology development and cross-disciplinary translational work in advanced and flexible microelectronics. He will also shed light on the Master of Science in Semiconductor Technology & Operations, underscoring SHINE's role in strengthening Singapore's semiconductor talent pipeline and supporting workforce readiness for industry needs.

Biography:

Prof Lim Yeow Kheng is the Programme Director of the SHINE Centre and the Master of Science in Semiconductor Technology and Operations (STO) programme at the National University of Singapore (NUS). He also serves as Assistant Dean (Research and Technology) and Professor in the Department of Electrical and Computer Engineering at the College of Design and Engineering. With over 20 years of industry experience in semiconductor technology and OSAT manufacturing, Prof Lim has held leadership roles at GlobalFoundries and JCET Group. His research interests span advanced wafer-level packaging, heterogeneous integration, nanomaterials, flexible electronics, and AI/ML applications. He is a Senior Member of IEEE, holds multiple patents, and is active in numerous local and international technical committees and conferences in microelectronics and packaging technologies.

Invited Talk 1

Two-Dimensional Materials as Platforms for Scalable Nanoelectronics and Monolithic-3D Integration

Kaustav Banerjee
Electrical and Computer Engineering Department
University of California, USA

Abstract:

As semiconductor technologies approach fundamental limits in scaling and energy efficiency, continued progress increasingly depends on materials and integration strategies beyond conventional silicon–copper platforms. Two-dimensional (2D) van der Waals materials—such as graphene and transition-metal dichalcogenides—offer unique properties that support operation at extreme dimensions and dense three-dimensional integration.

This talk presents a platform-level perspective on how 2D materials enable continued nano electronic scaling and monolithic three-dimensional integration. Emphasis is placed on device physics and predictive design frameworks governing contacts, electrostatics, interconnect resistivity, kinetic inductance, and power density.

The discussion focuses on physically realistic and manufacturable pathways for integrating 2D materials into transistors, beyond-copper interconnects, RF passives, and monolithic-3D architectures, drawing on advances from my research group and lab-to-fab translation efforts through Destination 2D, which I co-founded.

Biography:

Kaustav Banerjee is Professor of Electrical and Computer Engineering and Director of the Nanoelectronics Research Lab at the University of California, Santa Barbara. His research establishes two-dimensional (2D) materials as foundational platforms for scalable, energy-efficient nanoelectronics, spanning transistors, interconnects, RF passives, and monolithic three-dimensional integration. He is recognized for pioneering device-physics-driven frameworks that identify the fundamental limits of silicon–copper technologies and define practical pathways beyond them. His innovations have influenced industrial technology roadmaps, including advanced interconnect strategies, and are being translated through Destination 2D, which he co-founded.

Professor Banerjee is a Fellow of IEEE, APS, AAAS, JSPS, and AIIA, and a Clarivate Highly Cited Researcher. His international honors include the Humboldt Foundation Bessel Prize, the JSAP Fellow International title, and the IEEE Kiyo Tomiyasu Award. He received his Ph.D. in Electrical Engineering and Computer Sciences from the University of California, Berkeley.

Invited Talk 2

Optical Connectivity Technology Challenges in the AI Era

Prof Radha Nagarajan
Visiting Professor of NUS
SVP and CTO, Optical Engineering
Marvell Technology, Inc

Abstract:

The need for hyperconnectivity in large scale AI data centers is pushing the limits on size, power, and heterogeneous integration of optical components.

In this talk, we explore the challenges in designing increasingly complex, low power and high-speed optical interconnects for the Scale-Up, Scale-Out and Scale-Across applications.

Biography:

Dr Nagarajan is Senior Vice President and Chief Technology Officer of Marvell's Optical Engineering Group, where he leads the development of the company's optical platform products and technologies. He also serves as a Visiting Professor in the Department of Electrical and Computer Engineering at the National University of Singapore. He earned his B.Eng. from NUS, M.Eng. from the University of Tokyo, and Ph.D. from the University of California, Santa Barbara, all in Electrical Engineering.

Dr Nagarajan is a member of the National Academy of Engineering (US) and a Fellow of IEEE, Optica, and IET. His recognitions include the IEEE/LEOS Aron Kressel Award, the IPRM Award, and the Optica David Richardson Medal for pioneering contributions to photonic integrated circuits. He holds over 250 US patents.

.

Invited Talk 3

Strategic Directions for Electronics Packaging

Prof Subramanian S. Iyer
Distinguished Professor
Charles P. Reames Endowed Chair
Electrical Engineering Department
University of California, USA

Abstract:

Recent advances in electronics packaging have come to the rescue as CMOS scaling has stalled, enabling the remarkable progress in Artificial Intelligence and Machine Learning that promises to transform our lives. This journey, however, has only just begun, and much more is yet to come.

The key features driving this transformation can be summarized by the strategy of "scale-down and scale-out," which has characterized monolithic CMOS scaling for decades, combined with the shift to chiplets for higher yields and the ability to integrate diverse technologies on the same substrate. This approach blurs the line between a monolithic chip and a large heterogeneous assembly of chips.

While progress has been made, current technologies still rely heavily on legacy packaging methods, making such systems complex and expensive to build. In this talk, we will describe our approach to simplify packaging at all levels—including design, architecture, process, and manufacturing—with the potential to take packaging to the next level and enable systematic scalability.

There are many challenges in this approach. We will outline these challenges and demonstrate how adopting silicon-like technologies, new cooling and power delivery strategies, and advanced design enablement can propel packaging into the next dimension.

Biography:

Subramanian S. Iyer (Subu) is a Distinguished Professor at UCLA, holding the Charles P. Reames Endowed Chair in Electrical Engineering and a joint appointment in Materials Science and Engineering. He is the founding Director of the Center for Heterogeneous Integration and Performance Scaling (UCLA CHIPS). In 2023–24, he led the U.S. Department of Commerce's National Advanced Packaging Manufacturing Program, defining the strategic roadmap for advanced packaging technologies. Previously, he was an IBM Fellow recognized for pioneering breakthroughs in semiconductor devices and integration.

… To be cont'd

Invited Talk 3

His technical innovations include developing the world's first SiGe base heterojunction bipolar transistor (HBT), salicide processes, embedded DRAM, electrical fuses, and advancing the 45 nm technology node that enabled ultra-low power portable devices. He also led the commercialization of the first interposer and 3D integrated circuit products. His current research explores wafer-scale architectures, in-memory computing, and novel device paradigms for medical engineering. He is a Fellow of IEEE, APS, iMAPS, and NAI and recipient of the IEEE Daniel Noble Medal among other honors.

Invited Talk 4

The Backend Revolution –
How Advanced Packaging & Interconnect Redefines Microelectronics

Dr Alfred Yeo
Director, Research and Development
STATS ChipPAC

Abstract:

Backend revolution has transformed the way chips are interconnected, assembled, and tested, from a low-margin, commoditized step into a high-value engineering discipline that now determines system performance, power efficiency, and form factor. Key drivers of the revolution are mainly due to the upsurge of AI/ML workloads and the proliferation of edge & mobile devices. In the old paradigm, packaging was purely structural, protecting the chip, delivering a thermal dissipation path, and providing electrical connections to the board. It was standardized, cost-driven, and followed Moore's Law scaling. Shifting into a new paradigm, packaging is now an extension of silicon design process, enabling system-level integration when transistor scaling becomes challenging.

Advanced packaging is the answer to this new paradigm shift, where major technological innovation has been developed related to 2.XD integration, 3D stacking, Fan-Out Wafer-Level Packaging, Co-Package Optics, and Chiplet assemblies. Research in interconnection methods and materials employed in these technologies is critical for the future of advanced packaging solutions. In essence, the assembly backend revolution has set its sights on packaging as a primary driver of semiconductor innovation, enabling continued system scaling and specialization beyond the limits of monolithic silicon. It represents a paradigm shift from "Assembly & Interconnect for Silicon" to "Silicon for Assembly & Interconnect

Biography:

Dr Alfred Yeo is currently R&D Director at STATS ChipPAC, Singapore, with over 25 years of experience in the semiconductor industry. He has held key positions at Infineon, GlobalFoundries, and Advanced Micro Devices, contributing extensively to semiconductor packaging innovation.

His expertise spans chip-package interaction design, modeling and simulation, process engineering, assembly metrology, prototyping, reliability, and product life cycle management.

Dr Yeo holds a Ph.D., M.Eng., and B.Eng. (Hons) from Nanyang Technological University, Singapore.

Invited Talk 5

Memory Matters!
Advanced Packaging Roadmap for DRAM and NAND Enabling Heterogeneous Integration

Dr Shyam Surthi
Distinguished Member of Technical Staff
NAND Process Integration
Micron Technology, Inc

Abstract:

Generative AI has made memory—DRAM, NAND, and HBM—central to performance and data storage, driving rapid advances in packaging technology. This talk examines the shift from conventional packaging to TSVs and hybrid bonding and explores heterogeneous integration trends such as stacking and bonding for AI-centric architectures.

Micron's roadmap focuses on scaling stacked die and tightening 3D interconnect pitch to meet escalating performance demands. We will also address key challenges in materials, thermal and mechanical management, and inspection. By spotlighting breakthroughs and barriers in DRAM, NAND, and HBM packaging, this session offers a forward-looking view of memory's role in powering next-generation AI.

Biography:

Shyam Surthi is a Distinguished Member of Technical Staff in the Advanced NAND Technology team, currently based in Singapore. He holds a BS and MS in Chemical Engineering from the University Institute of Chemical Technology, Mumbai, India, and a Ph.D. in Electrical Engineering from the University of Alabama, where he specialized in the processing and characterization of perovskite materials. He subsequently conducted postdoctoral research at North Carolina State University, developing Si-molecular devices for memory applications.

Shyam joined Micron in 2004 in Diffusion Process Development, working on various film development projects before transitioning to Advanced DRAM Process Integration. Since 2011, he has held leadership roles in films process development for DRAM and emerging memory, as well as technical leadership roles in NAND pathfinding with a focus on integration.

He is a Senior Member of IEEE and the inventor on 72 U.S. patents and numerous international patents, with more than 25 publications in refereed technical journals and conference proceedings.

.

Invited Talk 6

Advanced Laser Integration and Packaging Technologies for High-Performance Silicon Photonic Modules

Dr Jack Sheng Kee
Senior Director, Silicon Photonics Business Division
Delta Electronics

Abstract:

The rapid advancement of silicon photonics for next-generation optical communication, LiDAR, and sensing systems demands precise, stable, and scalable laser sources across the O-, C-, and L-bands.

This presentation reviews the current landscape of semiconductor lasers—including distributed feedback (DFB) lasers, vertical-cavity surface-emitting lasers (VCSELs), external cavity lasers (ECLs), and emerging frequency combs—highlighting their spectral performance, modulation capabilities, and thermal stability for FMCW and coherent detection applications. We emphasize the critical role of integration and packaging techniques—such as polymer-based bonding, precision pick-and-place assembly, microlens coupling, and 3D-printed optical interfaces—in achieving low-loss, high-yield chip-to-chip coupling between III-V laser dies and silicon photonic circuits.

Furthermore, we discuss integrated control strategies for laser wavelength, output power, and thermal management, essential for maintaining phase coherence and linewidth stability in demanding applications.

Biography:

Dr Kee Jack Sheng is Senior Director of Delta's Advanced Technology Team and Head of Delta's Silicon Photonics Business Division, leading efforts to translate advanced silicon photonics into practical solutions for smarter, safer environments—from industrial machinery to intelligent everyday systems.

Under his leadership, the division develops integrated photonic chips and systems that power next-generation sensors and intelligent solutions, enhancing precision and responsiveness in robotics, autonomous systems, and digital twin applications.

Previously, Dr Kee led Delta's R&D in Cyber-Physical Systems, advanced sensors, communication, and intelligent control for Industry 4.0, including reconfigurable manufacturing and robotics. He also spearheaded Singapore's first mobile learning platform for Industry 4.0, leveraging AI and knowledge systems to deliver personalised, on-demand upskilling.

A strong advocate of continuous learning, Dr Kee emphasises that technological progress must be matched by human capability growth.

Workshop Speaker 1

What are Quantum Computers and What is the Role of Semiconductors in This Field

Prof Alberto Sangiovanni-Vincentelli
SHINE Thrust-1 Research Collaborator
University of California, USA

Abstract:

With the bulk of technology news these days centered around Artificial Intelligence (AI), it is easy to lose sight of other fast advancing technologies and trends. One such space is the field of quantum technologies. In this presentation, I will review the industrial landscape of quantum technology, from computing to communication, and then focus on quantum computing.

I will review the basic principles of quantum approaches to computation and the latest results on quantum algorithms and their limitation. I will then review the underlying basic physics solutions for quantum computers including photonic networks, superconducting circuits, spin qubits, neutral atoms, and trapped ions. I will then touch upon error correction as an essential piece of quantum computing use.

Biography:

Alberto Sangiovanni Vincentelli (Fellow) is the Edgar L. and Harold H. Buttner Chair of EECS at the University of California, Berkeley. He is author or co-author of over 1,000 papers, 17 books, and holds three patents in design tools, methodologies, large-scale and embedded systems, hybrid systems, and AI. He co-founded Cadence and Synopsys, the leading companies in Electronic Design Automation.

He is an IEEE and ACM Fellow and a member of the US National Academy of Engineering. He has served on advisory boards for companies including BMW, Intel, Mercedes, and STMicroelectronics, and currently serves on the boards of Cadence, KPIT Technologies, eGap, Exein, and Cy4Gate. He chairs Quantum Motion, Innatera, Phoelex, e4Life, and Phononic Vibes.

Prof. Sangiovanni Vincentelli has held leadership roles in the Italian National Science Foundation, the Italian Institute of Technology, and is President of Chips.it, a €250M Italian government initiative. His awards include the IEEE/RSE Wolfson James Clerk Maxwell Medal and the BBVA Frontiers of Knowledge Award.

Workshop Speaker 2

2D Materials Based Composites for Flexible Sensors and Thermal Management

Prof Lee Pooi See
SHINE Thrust-2 Co-Investigator
Nanyang Technological University

Abstract:

2D materials are versatile building blocks for flexible sensing and thermal management. We have developed continuous monolayer of Molybdenum Disulfide which delivers a linear piezoelectric response, attributed to the broken inversion symmetry in the single-layer structure. Bendable piezoelectric sensor based on this film exhibits high sensitivity, benchmarked against reported 2D binary semiconductors.

For thermal management, we have incorporated Boron Nitride nanosheets and liquid metal nanoparticles as thermally conductive fillers in a photocurable polydimethylsiloxane matrix to form a thermal interface material. This composite shows high thermal conductivity and an ultralow Young's modulus, enabling superior conformability on complex surfaces and minimizing thermal contact resistance.

Biography:

Prof Pooi See Lee is the President's Chair Professor in Materials Science & Engineering at Nanyang Technological University (NTU), Singapore.

Her research focuses on deformable electroactive composites for soft actuators, sensors, and energy devices, advancing the frontiers of smart materials and functional systems. She has received several prestigious recognitions, including the Nanyang Research Award (2016), the Nanyang Award for Innovation and Entrepreneurship (2018), and the NRF Investigatorship (2016).

Prof Lee is consistently recognized for her global research impact, being listed as a Highly Cited Researcher by Clarivate Analytics (2018–2024). She has also been honored with the SNIC–AsCA Distinguished Woman Chemist Award (2022), and is a Fellow of the National Academy of Inventors (2020), Materials Research Society (2022), and the Royal Society of Chemistry (2022).

Workshop Speaker 3

Advanced Materials and Interfaces for Heterogeneous Integration

Dr Li Yanzhen
SHINE Thrust-2 Research Fellow
Nanyang Technological University

Abstract:

Hybrid electronics are reshaping the landscape of modern electronic systems, enabling transformative applications in healthcare technologies, human–machine interfaces, and robotics, where performance, reliability, and scalability are critical to industrial adoption and deployment.

Our Thrust advances next-generation heterogeneous integration through materials-enabled innovations, bringing together functional materials, sensor technologies, and system-level design through coordinated interdisciplinary research. By harnessing intrinsic material properties and engineered interfaces, we directly address key industry-relevant challenges, including device integration, interconnect reliability, and thermal management in complex electronic systems. Our work positions materials innovation as a practical enabler of manufacturable, high-performance platforms than isolated components. Representative advances include robust interconnect materials for reliable electrical connections, liquid metal–based thermal management solutions for efficient heat dissipation, and sensor architectures designed for seamless integration into heterogeneous systems.

Together, these efforts support the development of scalable, reliable hybrid electronic technologies ready for real-world deployment and industrial translation.

Biography:

Li Yanzhen is a Research Fellow in the School of Materials Science and Engineering at Nanyang Technological University (NTU), where he also earned his Ph.D. He holds a B.Sc. in Materials Science and Physics from Nanjing University (NJU).

His research focuses on mechanical sensors and flexible electronic devices, with a particular emphasis on structure-driven design and system-level integration.

Workshop Speaker 4

SHINE Design Enablement and Innovation: Learnings from Chiplets to Methodologies

Prof Massimo Alioto
SHINE Thrust-1 Co-Investigator
National University of Singapore

Abstract:

During the course of the SHINE program, heterogeneous integration has taken the center stage in silicon system scaling, pushing traditional integration from board to substrate, design IP to chiplet, and single-vendor to multi-vendor chiplets. This talk focuses on SHINE design-to-testing (eco)system enablement for aggressive power and cost scaling down in high-mix low-volume manufacturing and illustrating innovation in all three dimensions.

From a design viewpoint, the SHINE chiplet ecosystem innovates system(atic) methodologies, many-chiplet and multi-vendor architectures, and massive simultaneous testing methodologies. For deployment in a wide range of substrates down to very limited routability, low-dimensional systems down to near-1D are enabled by the first bus providing all traditional system functions over a single wire. Several breakthrough silicon demonstrations are illustrated including the first systems-on-wire heterogeneous ecosystem, and multi-modal e-textiles with sub-100 pW consumption.

SHINE research cuts the last wire through wireless communications with >1,000X power reductions and 100-m range, as demonstrated by a new class of standard-compliant Bluetooth radios with μW power. The traditionally dominant testing cost in low-cost chiplet is reduced by orders of magnitude through the first probe-less and position-invariant testing framework for simultaneous massive testing of large chiplet batches (by the thousands). The underlying design methodologies are made accessible to the design ecosystem via the SHINE open Standard (SHINES), as exemplified by several silicon demonstrations with unprecedented levels of power and minimally-complex integration/testing.

Overall, the research output in Thrust 1 of the SHINE program lowers the barrier to entry and accelerates time-to-value both at the chiplet and the system integration level, creating new opportunities and economies of scale for local companies and global markets.

… To be cont'd

Workshop Speaker 4

Biography:

Massimo Alioto is Provost's Chair Professor in the Department of Electrical and Computer Engineering at the National University of Singapore, where he leads the Green IC Group and the Integrated Circuits and Embedded Systems area. He has held positions at the University of Siena, Intel Labs, the University of Michigan–Ann Arbor, UC Berkeley, and EPFL.

He is the (co-)author of over 400 journal and conference papers and four Springer books, with two more forthcoming. His research focuses on ultra-low-power and self-powered systems, green computing, circuits for machine intelligence, and hardware security. He has served as Editor-in-Chief of IEEE Transactions on VLSI Systems, Deputy Editor-in-Chief of IEEE JETCAS, and Chair of the IEEE CAS Distinguished Lecturer Programme. He is an IEEE Fellow.

Workshop Speaker 5

Thermal Management Solutions for Flexible Antenna Arrays

Dr Jiang YiZhou
SHINE Thrust-3A Research Fellow
National University of Singapore

Abstract:

Implementing active antenna systems on flexible substrate leads to increased functionality and decreased form factors, while squeezing more power into compact packages. As a consequence, thermal management has become more critical for successful deployment of these systems.

On this workshop, we will share our approach on thermal management for flexible antenna systems, including passive and active methods.

Biography:

Dr Yizhou Jiang is a Research Fellow at the Singapore Hybrid-Integrated Next-Generation µElectronics Centre. He earned his Ph.D. in 2023 from the School of Information Science and Technology, Fudan University, China.

His research focuses on co-design, hybrid integration, and optimization of solid-state circuits in combination with flexible electronics and emerging devices.

Dr Jiang joined the National University of Singapore in 2023.

Workshop Speaker 6

Flexible Phased Array Demonstrators

Prof Koenraad Mouthaan
SHINE Thrust-3B Co-Investigator
National University of Singapore

Abstract:

The research and development of innovative, flexible and conformable antennas for application in phased arrays for communication and remote sensing systems is one of the key objectives of the SHINE program. In this presentation, the design, fabrication, and testing results of several flexible phased arrays are presented. Integration of active components, such as power amplifiers, will be presented as well.

Biography:

Koen Mouthaan received the M.Sc. and Ph.D. degrees in electrical engineering from Delft University of Technology in the Netherlands. He worked at TNO Defense, Safety and Security in the Netherlands, and at SkyGate, a company that designed phased-array antennas for consumer applications.

Between 2003 and 2015 he was assistant professor and tenured associate professor in the Department of Electrical and Computer Engineering at the National University of Singapore. He rejoined the same department in 2016. His research interests include microwave and millimeter-wave circuits and systems, phased array antennas, digital beamforming, and design and innovation.

He also holds an MBA from Nanyang Technological University, a MSc in organizational leadership from Johns Hopkins University, and a Master in Space Engineering from the Technical University of Berlin.

Workshop Speaker 7

Design and Development of the Si/SIC Interposer

Dr Lim Teck Guan
Senior Scientist (System-in-Package)
A* STAR IME

Abstract:

Integrating high-performance III–V RF MMICs with advanced-node CMOS processors for Edge AI and next-generation RF front-end systems presents significant challenges in thermal management, signal integrity, and packaging reliability. These systems require compact cooling solutions, robust mechanical performance, and high-frequency, high-bandwidth interconnects to support increasingly dense, high-power-dissipation circuits.

Among available approaches, the 2.5D interposer platform based on silicon (Si) or silicon carbide (SiC) is well suited to meet these requirements, offering high-density, wide-bandwidth interconnects, low-loss impedance-controlled RF signal lines, and high thermal conductivity for efficient heat dissipation from active devices such as RF power amplifiers. Conventionally, the interposer is assembled onto a printed circuit board (PCB) or substrate using ball grid array (BGA) interconnections, which provide system-level electrical connectivity and thermal paths. Underfill is typically applied between the BGA joints to reduce thermomechanical stress and enhance solder joint reliability.

In this work, a novel 2.5D interposer-to-PCB integration architecture incorporating a backside patterned Cu–Mo interface layer is presented. The Cu–Mo layer provides high thermal conductivity, extends solder joint lifetime through improved thermomechanical compliance, and mitigates RF interference by introducing a controlled electromagnetic return and shielding path. This architecture effectively overcomes key limitations of conventional BGA-based interposer-to-PCB or substrate integration schemes, enabling a compact, thermally efficient, and mechanically reliable packaging solution for high-power and high-frequency heterogeneous integration.

Biography:

Teck Guan is a Principal Scientist and Team Lead of the System-in-Package Research Group at IME. His research focuses on advanced packaging and integration for RF, millimeter-wave, and photonic circuits

Workshop Speaker 8

3D-Printed Micro-Optics for Laser Chip Packaging and Integration

Dr Chua Yun Da
SHINE Thrust-4 Research Fellow
National University of Singapore

Abstract:

The integration of laser sources into photonic systems remains a critical challenge for achieving scalable and high-performance photonic integration. Two-photon polymerization (2PP) 3D printing provides a flexible hybrid integration approach by enabling the direct fabrication of freeform optical and mechanical structures across dissimilar photonic platforms.

This technique allows versatile integration of both edge and surface emitting devices, offering relaxed packaging tolerances and minimal wavelength dependency compared to conventional grating couplers.

This presentation reviews recent advances in light source integration and highlights how 2PP-enabled approaches compare with existing integration strategies.

Biography:

Dr Chua Yun Da received his PhD in 2025 from Nanyang Technological University (NTU), where he focused on topological lasers in the terahertz (THz) spectrum. His doctoral research, conducted in collaboration with the Institute of Materials Research and Engineering (IMRE), encompassed simulation, fabrication, and experimental characterization of advanced photonic devices.

Currently, Dr Chua's work centres on hybrid photonic integration, aiming to develop scalable and manufacturable photonic systems for next-generation technologies.


NUS
National University
of Singapore
College of Design
and Engineering
SHINE
Singapore Hybrid-Integrated
Next-Generation μ-Electronics Centre